Nicole C. Rodia

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Education

PhD **Stanford University**, Stanford, California
Electrical Engineering, expected June 2016, GPA: 3.68

MS **Stanford University**, Stanford, California
Electrical Engineering, June 2011, GPA: 3.40

BS **Cornell University**, Ithaca, New York
Electrical and Computer Engineering, May 2009, GPA: 3.55
Graduation with honors.

Relevant Coursework

Advanced Computer Architecture, Computer System Architecture, Parallel Programming and Computer Architecture, Social and Information Network Analysis, Digital VLSI Design, Digital Logic Design, Computer Networks, Microelectronics, Control System Design, Mechatronics, Digital Design with Microcontrollers

Research Experience

Graduate Research Assistant, *Pervasive Parallelism Lab, Stanford University*
Jan. 2011-present
research advisor: Prof. Kunle Olukotun

- Characterizing parallel graph analysis algorithms to understand performance on parallel architectures
- Designing memory controller and cache-based hardware optimizations for graph algorithms

Graduate Research, *Department of Computer Science, Stanford University*
Mar. 2010-Jun. 2010
research advisor: Prof. Sebastian Thrun

- Developed algorithm for detecting and counting steps during human walking using a hand-held cellphone accelerometer
- Combined step-based motion model with Wi-Fi data for indoor pedestrian localization

Undergraduate Research Assistant, *Department of Theoretical & Applied Mechanics, Cornell University*
Jan. 2008-May 2009
research advisor: Prof. Andy Ruina

- Designed electronic hardware system, including component selection, circuit design, and printed circuit board layout, for walking robot, Cornell Ranger, which set a 23 km walking record in July 2010
- Implemented and tested software PID motor current controller for use with Cornell Ranger

Professional Experience

Research Intern, *Intel Labs, Accelerator Architecture Lab, Hillsboro, OR*, Summer 2014
- Characterized parallel graph analysis framework applications on x86 multicore architectures

PhD Research Intern, *Pacific Northwest National Laboratory (PNNL)*, Richland, WA, Summer 2012
- Simulated GPU architectures to study performance of irregular and communication-intensive applications

Software Engineering Intern, *Google*, Mountain View, CA, Summer 2011
- Network protocol experiments & hardware component evaluation for network-attached hardware prototype
- Datacenter server and prototype reliability analysis and documentation

Technical Intern*, Advanced Silicon Technology Group, MIT Lincoln Laboratory*, Lexington, MA, Summers 2009 & 2010
- Designed digital logic in VHDL for FPGA-based control of digital focal plane array readout integrated circuit (DFPA ROIC) infrared imager
- Constructed and performed wafer-based tests on DFPA ROIC
- Documented custom ROIC design, including implementation details & functional schematics
- Designed full-custom CMOS layout for digital counter in infrared imager ROIC

Circuit Design Co-op, *Advanced Micro Devices*, Sunnyvale, CA, Fall 2007 & Summer 2008
- Designed physical circuits including gate sizing, timing, placement, and schematic drawing
- Ran and debugged logical equivalency checking on multiple circuits
- Analyzed noise, electromigration, power consumption, and timing of circuits using CAD tools

Project Engineering Intern, *Perrigo Company*, Allegan, MI, Summer 2006
- Managed pharmaceutical manufacturing and packaging equipment projects, including initiation, timeline planning, appropriation requests, and task coordination
- Updated optical character verification vision system software

Website Technician, *Cornell University Campus Life*, Ithaca, NY, Sep. 2005-Aug. 2007
- Designed and maintained the official Cornell Campus Life Website pages

Analytical R&D Lab Intern, *Perrigo Company*, Allegan, MI, Summer & Winter 2005
- Performed stability tests on pre-production drug products in FDA-regulated laboratory
- Developed testing procedures for new products

Teaching Experience

Academic Consultant, Computer Organization Course, *Cornell University,* Spring 2009
- Assisted students with projects and assignments for junior-level course
- Held regular office hours

Presentations

- S. Hong, N. Rodia, K. Olukotun, "On Fast Parallel Detection of Strongly Connected Components (SCC) in Small-World Graphs", *SC '13*, Denver, CO, Nov. 2013.

Presentations, continued
- N. Rodia and K. Oluktoun, "A Simulation-Based Study of Graph Algorithm Characteristics," *Oracle Labs*, Redwood Shores, CA, May 2012.
- N. Rodia, "Accelerometer-Based Pedometry for Indoor Localization." *Qualcomm Innovation Fellowship Presentation*, Qualcomm Research & Development, Santa Clara, CA, Oct. 2010.
- N. Rodia, E. Le Grand, A. Atreya, "Indoor Localization Using Cell Phone Sensors." *Qualcomm Innovation Fellowship Presentation*, Qualcomm Research & Development, Santa Clara, CA, Apr. 2010.
- N. Rodia, "DFPA Technology." *MIT Lincoln Laboratory Internship Program*, MIT Lincoln Laboratory, Lexington, MA, Aug. 2009.

Papers
- S. Hong, N. Rodia, K. Olukotun, "On Fast Parallel Detection of Strongly Connected Components (SCC) in Small-World Graphs", *SC '13,* Denver, CO, Nov. 2013.

Posters
- N. Rodia and K. Olukotun, "Characterizing Parallel Social and Information Network Analysis Algorithms," *Army High Performance Computing Research Center (AHPCRC) Booth, SC '13,* Denver, CO, Nov. 2013.
- N. Rodia and K. Olukotun, "A Simulation-Based Study of Graph Algorithm Characteristics," *PPL Retreat,* San Francisco, CA, Jun. 2012.
- T. Oguntebi, N. Rodia, and K. Olukotun, "A Data-Centric Parallel Architecture for High Performance Graph Processing," *PPL Retreat,* Half Moon Bay, CA, Jun. 2012.
- N. Rodia, S. Lee, and J. Liu, "Cornell Ranger: Walking Robot Electronics System Design." *Cornell Undergraduate Research Board Spring Research Forum*, Cornell University, Ithaca, NY, Apr. 2009.

Awards and Fellowships

Stanford University Lyman D. Austin Engineering Fellowship, Sep. 2009
- Five-quarter fellowship award based on academic achievement

SWE General Electric Women's Network Scholarship, Aug. 2007
Intel Foundation Scholarship, May 2007

Professional Affiliations

Webmaster, Member & Volunteer, *Stanford Women in Electrical Engineering*, Sep. 2009-Present
Member, *Institute of Electrical and Electronics Engineers (IEEE)*, Sep. 2009-Present
Member, *Association for Computing Machinery (ACM)*, Jul. 2012-Present
Event Director & Volunteer, *Society of Women Engineers*, Aug. 2005-Jun. 2012

University Service

Volunteer Teacher, *Stanford ESP Splash! Sessions,* Apr. & Nov. 2010-2014

Skills

Programming: C/C++, Python, Matlab/Simulink, Java, Verilog
ECAD: Cadence Virtuoso, Eagle PCB Design

Professional Training

Intern Engineer, *State of New York,* Aug. 2009