Nicole C. Rodia

nrodia@stanford.edu www.nicolerodia.com

Education

Stanford University, Ph.D. Candidate, Electrical Engineering, 3.68 GPA **6/2011-Present**
Stanford University, M.S., Electrical Engineering, 3.40 GPA **6/2011**
Cornell University, B.S., Electrical & Computer Engineering, *Cum Laude*, 3.55 GPA **5/2009**

Research and Technical Experience

- **Research Assistant** **1/2011-Present**
  Stanford University, Pervasive Parallelism Laboratory, Stanford, CA Advisor: Professor Kunle Olukotun
  - Designing cache and memory optimizations to improve parallel graph algorithm performance
  - Analyzed performance and data locality of parallel graph algorithms on multicore architectures using:
    - Zsim multicore performance simulator; implemented additional cache measurements (C++)
    - Processor performance counters using Performance API (PAPI) and Intel PCM
    - Reuse distance algorithm with partial sum optimization (C++)
  - Helped implement and evaluate a parallel strongly connected components (SCC) algorithm for small-world graphs; 5-29x speedups over sequential algorithm on 32 thread system [Hong, *Rodia*, Olukotun; SC'13]
- **Research Intern** **6/2014-9/2014**
  Intel Labs, Accelerator Architecture Lab, Hillsboro, OR
  - Characterized parallel graph analytics framework apps using CPU performance counters (Intel VTune)
  - Identified inefficiencies in PageRank algorithm for GraphLab and Green-Marl analytics frameworks
- **Research Intern** **6/2012-9/2012**
  Pacific Northwest National Laboratory (PNNL), High Performance Computing Group, Richland, WA
  - Studied performance of irregular and communication-intensive applications using GPGPU-Sim simulator
  - Evaluated tradeoff between cache size and thread contexts; found performance benefit for L2 cache
- **Software Engineering Intern** **6/2011-9/2011**
  Google Research, Mountain View, CA
  - Evaluated feasibility and performance of datacenter prototype device using networking experiments, component evaluation, and datacenter server and prototype reliability analysis
- **Research Intern** **6/2010-9/2010**
  MIT Lincoln Laboratory, Advanced Silicon Technology Group, Lexington, MA **6/2009-9/2009**
  - Designed full-custom CMOS layout for digital counter in infrared imager readout integrated circuit (ROIC)
  - Performed FPGA and wafer-based tests on infrared imager ROIC test chip to determine functionality
  - Documented custom ROIC design, including implementation details and functional schematics
- **Circuit Design Co-op** **5/2008-8/2008**
  Advanced Micro Devices (AMD), Sunnyvale, CA **8/2007-12/2007**
  - For next-generation x86-64 microprocessor chip:
    - Designed physical circuits, including gate sizing, timing, placement, and schematic drawing
    - Evaluated RTL and circuit logical equivalence; analyzed noise, electromigration, power, and timing

Programming Languages: C/C++, Python, Matlab, Verilog

University Service

- **Stanford Women in Electrical Engineering**, *Webmaster, Board Member* **9/2010-9/2015**
- **Stanford Splash! Program**, *Volunteer Teacher (8 sessions)* **4/2010-4/2014**